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APPLICANT(S): Juha M. HEIKKILA
SERIAL NO.: 09/891,726
FILING DATE: 6/26/2001
EXAMINER: Unknown
DOCKET NO.: 872.0043.USU
TITLE: Circuit and Method for Correcting Clock Duty Cycle

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to Sections 609 and 707.05(b) of the MPEP and 37 CFR 1.97-1.99, copies are herewith submitted of documents which may be pertinent to the invention as claimed in the above-identified application. The attached form PTO-1449 lists these documents.

The citation of these documents should not be construed as a representation that a thorough search has been made, or that other, more pertinent material is not available.

Respectfully submitted,

Harry F. Smith
Reg. No. 32,493

HARRINGTON & SMITH, LLP
1809 Black Rock Turnpike
Fairfield, CT 06432

Telephone: (203)366-4084
Facsimile: (203)366-4109
email: hsmith@HSpatent.com
Customer No.: 29683



2

CERTIFICATE OF MAILING

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November 8, 2001

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Name of person mailing correspondence

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**INFORMATION DISCLOSURE
CITATION FORM FOR
PATENT APPLICATION
(FORM PTO-1449)
(Substitute)**

Docket No.: 872.0043/USU

Serial No.: 09/891,726

Applicant(s): Heikkila

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Group: 2661

U.S. PATENTS

Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date
					Technology Center 2600	RECEIVED JAN 11 2002

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a

OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)

	"ASMD With Duty Cycle Correction Scheme For High-Speed DRAM"; Jang, S. et al; Electronic Letters; Vol. 37, Issue 16; August 2, 2001; pp. 1004-1006
	"The Anti Jitter Circuit for the Suppression of Wideband Phase-Noise"; Underhill, M.J.; IEEE Colloquium on Microwave and Millimeter-Wave Oscillators and Mixers (Ref. No. 1998/480); December 1, 1998; pp. 2/1-2/14
	"Sampling Jitter in High-Speed SI Circuits.pdf"; Jonsson, B.E.; IEEE International Symposium on Circuits and Systems; Vol. 1; 1998; pp. 524-526
	"Effect Of Sample Clock Jitter On IF-Sampling IS-95 Receivers.pdf"; Stewart, K.A.; The 8 th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications; Vol. 2; 1997; pp. 366-370
	"Design Of High-Speed, Low Power Frequency Dividers And Phase-Locked loops in Deep Submicron CMOS"; Razavi, B. et al; IEEE Journal of Solid State Ciruits; Vol. 30, No. 2; February, 1995; pp.101-109

Examiner's Signature:

Date Considered:

Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered.
Include a copy of this citation form with your next correspondence to the Applicant(s).